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D. Remarks

Rejection of Claims 10, 14-16 and 19 Under 35 U.S.C. §102(a) based on Applicants' Background Art (*Background Art*).

The invention of amended claim 10 is directed to a method of forming a monitoring structure. The method includes etching a first process layer to form monitor trenches that extend through the first process layer and stop at an etch stop layer on a monitor wafer. The method also include forming a feature in, with, or in relation to the monitor trenches, wherein a process to be monitored with said monitor structure forms a corresponding non-monitor trench in a different process layer than the first layer.

As is well known, a claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single reference.

As can be understood from above, Applicants' claim 10 recites "etching a first process layer to form monitor trenches that extend through the first process layer". Such a limitation is not shown in the *Background Art*. To show such a limitation, the rejection argues the following:

> [The *Background Art*] method comprises etching a first layer 802 to form monitor trenches...[1]

However, as shown in the illustration below, the first layer 802 of Applicants' invention is never etched and does not include any trenches.

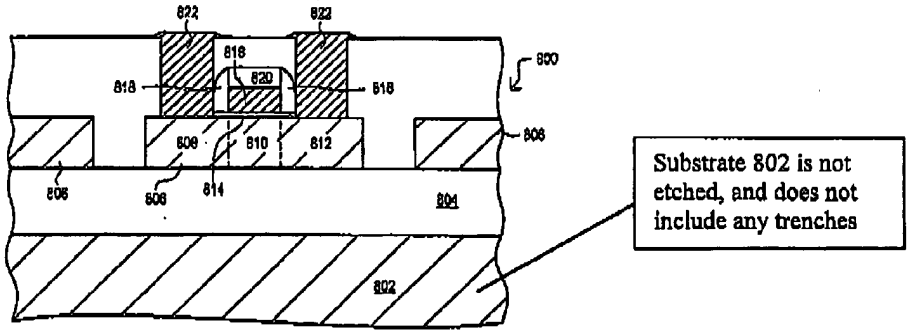

FIG. 8

[1] See the Final Office Action, dated 11/18/2003, Page 2, Section 2.

Thus, Applicants' SOI example of the *Background Art* does not show the etching of a first layer (802) whatsoever, let alone etching to form trenches that extend through the first layer (802).

If the rejection includes a typographical error, and it is being argued that silicon islands 806 correspond to a "first layer", the limitations of amended claim 10 are still not met. As noted above, FIG. 8 is a conventional SOI monitoring structure. As Applicants' Specification indicates, in such a conventional arrangement, a process to be monitored forms features in the same process layers as the monitoring structure.

> In the particular example of FIG. 8, such features may include a transistor... channel region... drain region... a gate dielectric... a gate... surrounding gate sidewalls... a gate top insulator... contacts... Such features, and others not mentioned here, can be monitored by viewing a conventional monitoring structure 800 in cross section.[2]

That is, in the example of FIG. 8, structures of a conventional SOI monitoring structure are essentially identical to non-monitor structures formed by a monitored process. Consequently, to monitor the SOI process, conventionally an SOI wafer must be destroyed.

> A drawback to such a conventional approach is that in order to monitor various SOI features an SOI wafer must typically be destroyed. Because SOI wafers are expensive, this can add expense to a manufacturing/development operation.[3]

As a result, if a spacing between silicon islands 806 is to be considered a "trench" formed in a layer of silicon islands 806, the process to be monitored forms a trench the very same process layer as the monitoring structure. This is contrary to Applicants' claim 10 limitations, in which a non-monitor trench is formed in a different process layer.

Thus, because the cited reference does not show all limitations of claim 10, this ground for rejection is traversed.

Claim 14, which depends from claim 10, includes additional claim limitations not shown or suggested by the *Background Art*. Claim 14 recites that the step of etching a first layer

[2] Applicants' Specification, Page 5, Lines 14-19, emphasis added.
[3] Applicants' Specification, Page 5, Lines 20-22.

includes forming a substrate trench etch mask. Such a limitation is shown or suggested by the example of FIG. 8 in Applicants' *Background Art*. As noted above, a trench is never etched in FIG. 8, thus a trench etch mask is not formed.

Still further, Applicants' Claim 15, which depends from claim 10, has additional limitations not shown in the cited reference. Nothing in the reference shows or describes an etch mask that essentially matches an SOI wafer island isolation pattern. The *Background Art* shows but one etch mask, and the etch mask matches a shallow trench isolation pattern, not any SOI island isolation pattern.[4]

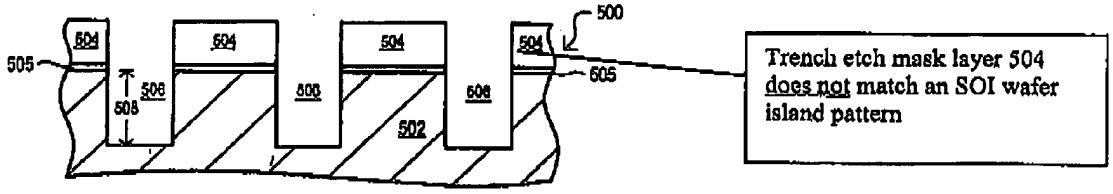

FIG. 5B

For all of these reasons, the *Background Art* is not believed to show all limitations of Applicants' claims, and this ground for rejection is traversed.

Rejection of Claims 20 and 23-25 Under 35 U.S.C. §102(a) based on the *Background Art*.

The invention of claim 20 is directed to a method of monitoring a semiconductor manufacturing process. The method includes processing a monitor wafer having monitoring trenches formed in a first process layer of the monitoring wafer according to at least one process step that forms a feature, the feature being formed in a non-monitoring wafer in, with, or in relation to a different process layer than the first process layer in the semiconductor manufacturing process.

To address this ground of rejection, Applicants incorporate by reference herein the same general comments set forth above for claim 10. Namely, that the *Background Art* does not show a monitor wafer with monitoring trenches in one process layer that monitors a process that forms a feature in a different process layer. As shown in Applicants' Specification, in the *Background*

[4] See Applicants' Specification, FIGS. 5A and 5B.

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Art example of FIG. 8, the SOI process is monitored by forming features in the same process layers on a monitor wafer, and then viewing the monitor wafer in cross section (thereby wasting an SOI wafer).

For these reasons, this ground for rejection is also traversed.

Applicants' amendments are believed to address the rejection's interpretation of Applicants' claims set forth in the Final Office Action. In particular, in addressing Applicants' previous showing, the rejection noted the following:

> Broadly interpreted, the first layer on the monitor wafer and the first layer on other wafers are separate and distinct layers...[5]

By reciting a first process layer and different process layer, the claims are now believed to be clearly distinguishable from such an interpretation.

Claims 10 and 20 have been amended. The present claims 10-26 are believed to be in allowable form. It is respectfully requested that the application be forwarded for allowance and issue.

Respectfully Submitted,

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[5] See the Final Office Action, Page 4, Lines 8-10.